AMENDMENTS TO THE CLAIMS

This listing of the claims will replace all prior versions, and listing, of claims in the application:

LISTING OF CLAIMS

1-26. (Cancelled)

27. (Previously Presented) A memory device comprising:

at least one synchronously controlled global element; and

a plurality of self-timed local elements, wherein at least one of said self-timed local elements interfaces with said synchronous controlled global element.

28. (Previously presented) The memory device of Claim 27, wherein said at least one synchronously controlled global element includes a global predecoder.

29. (Previously presented) The memory device of Claim 27, wherein said at least one synchronously controlled global element comprises at least one global decoder.

30. (Previously presented) The memory device of Claim 27, wherein said at least one synchronously controlled global element comprises at least one global controller.

31. (Previously Presented) The memory device of Claim 27, wherein said at least one synchronously controlled global element comprises at least one global sense amplifier.

32. (Previously Presented) The memory device of Claim 27, wherein said plurality of self-timed local elements comprises a plurality of memory cells forming at least one cell array.

33. (Previously Presented) The memory device of Claim 27, wherein said plurality of self-timed local elements comprises at least one local decoder.

34. (Previously Presented) The memory device of Claim 27, wherein said plurality of self-timed ~~ecal~~ local elements comprises at least one local sense amplifier.

35. (Previously Presented) The memory device of Claim 27, wherein said plurality of self-timed local elements comprises at least one cluster.

36. (Previously Presented) The memory device of Claim 27, wherein said plurality of self-timed local elements comprises at least one block.

37. (Previously Presented) The memory device of Claim 27, wherein said block comprises at least one sub-block.

38. (Previously Presented) The memory device of Claim 27, wherein said plurality of self-timed local elements comprise:

a plurality of memory cells forming at least one cell array;

at least one local decoder interfacing with said at least one cell array;

at least one local sense amplifier interfacing with said local decoder and said cell array and adapted to precharge and equalize at least one line coupled thereto; and

at least one local controller interfacing with and coordinating at least said local decoder and sense amplifier.

39. (Previously Presented) The memory device of Claim 38, wherein said plurality of self-timed local elements further comprise at least one cluster.

40. (Previously Presented) The memory device of Claim 27 comprising a plurality of synchronous controlled global elements.

41. (Previously Presented) The memory device of Claim 40, wherein at least two of said self-timed local elements interface with at least two different synchronous controlled global elements.

42. (Currently Amended) A synchronous self-timed memory structure comprising:

a plurality of memory cells forming at least one cell array;

at least one self-timed local decoder interfacing with said at least one cell array;

at least one self-timed local sense amplifier interfacing with at least said one self-timed ~~controlled~~ local decoder and said cell array and adapted to precharge and equalize at least one line coupled thereto; and

at least one self-timed local controller interfacing with and coordinating said self-timed local decoder and said self-timed sense amplifier.

43. (Previously Presented) The memory structure of Claim 42, further including at least one line replicating a global bit line interfacing with said self-timed local controller.

44. (Previously Presented) The memory structure of Claim 42, wherein said self-timed local sense amplifier is adapted to multiplex at least two sense amplifiers.

45. (Previously Presented) The memory structure of Claim 42, wherein said self-timed local sense amplifier is adapted to multiplex four sense amplifiers to a multiplexed line coupled to said self-timed local sense amplifier.

46. (Previously Presented) A synchronous controlled hierarchical memory structure that comprises a logical portion of a larger memory device, the hierarchical memory structure comprising:

a plurality of memory cells forming at least one cell array;

at least one self-timed local decoder interfacing with said at least one cell array;

at least one self-timed local sense amplifier interfacing with said at least one self-timed local decoder and said at least one cell array and adapted to precharge and equalize at least one line coupled thereto; and

at least one self-timed local controller interfacing with and coordinating said at least one self-timed local decoder and said at least one self-timed local sense amplifier.

47. (Previously Presented) A method of performing a read operation using a synchronous controlled memory device containing at least one logical memory subsystem, the method comprising:

selecting at least one cell array;

selecting at least one sub-block in the logical memory subsystem;

isolating at least one self-timed local sense amplifier;

activating a local wordline;

discharging at least one bitline in at least one bitline pair;

developing a differential voltage across said bitline pair;

stopping said discharge; and

equalizing and precharging said bitline pair.

48. (Previously Presented) The method of Claim 47, further comprising activating at least one mux line to select said cell array.

49.-50. (Cancelled)

51. (Previously Presented) A method of performing a write operation using a memory device containing at least one logical memory subsystem, the method comprising:

a global controller receiving data transmitted on at least one write bank line;

transmitting a high signal on a local word line; and

selecting at least one memory cell.

52. (Previously Presented) A method of performing a write operation using a memory device containing at least one logical memory subsystem, the method comprising:

a global sense amp receiving data transmitted on at least one write bank line;

transmitting a high signal on a local word line; and

selecting at least one memory cell.

53. (Previously Presented) A method of performing a write operation using a memory device containing at least one logical memory subsystem, the method comprising:

receiving data transmitted on at least one write bank line;

transmitting a high signal on a local word line; and

selecting at least one memory cell, wherein data to be written in said selected memory cell is put onto a global bit line synchronously with said at least one local write bank line.

54. (Previously Presented) The method of Claim 51 wherein data to be written in said selected memory cell is put onto a global bit line synchronously with said at least one local write bank line.

55. (Previously Presented) The method of Claim 51 comprising requesting the write operation.

56. (Previously Presented) The method of Claim 51 comprising preparing for a next access.

57. (Previously Presented) The method of Claim 56 wherein preparing for said next access comprises precharging at least one bit line.

58. (Previously Presented) The method of Claim 51 wherein said memory cell comprises at least one SRAM memory cell.

59. (Previously Presented) The method of Claim 51 wherein said memory cell comprises at least one DRAM memory cell.

60. (Previously Presented) The method of Claim 51 wherein said memory cell comprises at least one ROM memory cell.

61. (Previously Presented) The method of Claim 51 wherein said memory cell comprises at least one PLA memory cell.

62. (Previously Presented) The method of Claim 52 wherein data to be written in said selected memory cell is put onto a global bit line synchronously with said at least one local write bank line.

63. (Previously Presented) The method of Claim 52 comprising requesting the write operation.

64. (Previously Presented) The method of Claim 52 comprising preparing for a next access.

65. (Previously Presented) The method of Claim 64 wherein preparing for said next access comprises precharging at least one bit line.

66. (Previously Presented) The method of Claim 52 wherein said memory cell comprises at least one SRAM memory cell.

67. (Previously Presented) The method of Claim 52 wherein said memory cell comprises at least one DRAM memory cell.

68. (Previously Presented) The method of Claim 52 wherein said memory cell comprises at least one ROM memory cell.

69. (Previously Presented) The method of Claim 52 wherein said memory cell comprises at least one PLA memory cell.

70. (Previously Presented) The method of Claim 53 comprising requesting the write operation.

71. (Previously Presented) The method of Claim 53 comprising preparing for a next access.

72. (Previously Presented) The method of Claim 71 wherein preparing for said next access comprises precharging at least one bit line.

73. (Previously Presented) The method of Claim 53 wherein said memory cell comprises at least one SRAM memory cell.

74. (Previously Presented) The method of Claim 53 wherein said memory cell comprises at least one DRAM memory cell.

75. (Previously Presented) The method of Claim 53 wherein said memory cell comprises at least one ROM memory cell.

76. (Previously Presented) The method of Claim 53 wherein said memory cell comprises at least one PLA memory cell.

77. (Previously Presented) The method of Claim 53 comprising pulling down said at least one local write bank line at the same time as said global bit line.

78. (Previously Presented) The method of Claim 77 comprising pulling down said at least one local write bank line at a faster rate than said global bit line.

79. (Previously Presented) The memory device of Claim 27 wherein the memory device comprises an SRAM memory device.

80. (Previously Presented) The memory device of Claim 27 wherein the memory device comprises a DRAM memory device.

81. (Previously Presented) The memory structure of Claim 42 wherein said plurality of memory cells comprise at least one SRAM memory cell.

82. (Previously Presented) The memory structure of Claim 42 wherein said plurality of memory cells comprise at least one DRAM memory cell.

83. (Previously Presented) The memory structure of Claim 42 wherein said plurality of memory cells comprise at least one ROM memory cell.

84. (Previously Presented) The memory structure of Claim 42 wherein said plurality of memory cells comprise at least one PLA memory cell.

85. (Previously Presented) The memory structure of Claim 46 wherein said plurality of memory cells comprise at least one SRAM memory cell.

86. (Previously Presented) The memory structure of Claim 46 wherein said plurality of memory cells comprise at least one DRAM memory cell.

87. (Previously Presented) The memory structure of Claim 46 wherein said plurality of memory cells comprise at least one ROM memory cell.

88. (Previously Presented) The memory structure of Claim 46 wherein said plurality of memory cells comprise at least one PLA memory cell.

89. (Previously Presented) The method of Claim 47 wherein the memory device comprises a SRAM memory device.

90. (Previously Presented) The method of Claim 47 wherein the memory device comprises a DRAM memory device.